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09/989,762	11/19/2001	Kenneth Y. Ogami	CYPR-CD01175M	2087

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EXAMINER	
OSBORNE, LUKE R	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,762	OGAMI ET AL.	
	Examiner	Art Unit	
	Luke Osborne	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. Claims 1-33 have been presented for reconsideration. No claims have been added or cancelled. Claims 1-33 are now pending in the instant application.

2. Applicants' arguments submitted 12/15/2005 have been fully considered, Examiners response is as follows.

Examiner Notes

3. Examiner has become aware of PSoC Designer IDE User Guide version 1.09 5/30/2001 from Cypress MrcroSystems along with various other documents from Cypress related to the specified invention. Applicant is respectively reminded of their duty to disclose under 37 C.F.R 1.56. Examiner notes the lack of an Information Disclosure Statement in this case.

Drawings

4. Examiner acknowledges the replacement drawings for figures 1-5. Consequently the objection is withdrawn.

Abstract

5. Examiner acknowledges the amendment to the abstract. Consequently the objection is withdrawn.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-14 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

To be statutory, a claimed computer-related process must either:

(A) result in a physical transformation outside the computer for which a practical application in the technological arts is either disclosed in the specification or would have been known to a skilled artisan (discussed in i) below), or

(B) be limited to a practical application within the technological arts (discussed in ii) below) [MPEP 2106 IV B 2 (b)].

The term "practical application" means to manufacture in the case of a composition or product, to practice in the case of a process or method, or to operate in the case of a machine or system; and, in each case, under such conditions as to establish that the invention is being utilized and that its benefits are to the extent permitted by law or Government regulations available to the public on reasonable terms [35 USC 201 (f)].

Claim 1, as exemplary of claims 2-14, does not recite a physical transformation outside of a computer therefore, there is always some form of physical transformation within a computer because a computer acts on signals and transforms them during its operation and changes the state of its components during the execution of a process.

Even though such a physical transformation occurs within a computer, such activity is not determinative of whether the process is statutory because such transformation alone does not distinguish a statutory computer process from a nonstatutory computer process. What is determinative is not how the computer performs the process, but what the computer does to achieve a practical application [MPEP 2106 IV (B) (2) (b) (ii)].

A claim is limited to a practical application when the method, as claimed, produces a concrete, tangible and useful result; i.e., the method recites a step or act of producing something that is concrete, tangible and useful [MPEP 2106 IV (B) (2) (b) (ii)].

As such, the terminal step of Claim 1 "*identifying a first allowed programmable hardware resource...* " does not provide such a result. Merely identifying a resource does not qualify for statutory subject matter, rather something needs to happen to that result, i.e. the identified result becoming part of the design.

Any claim not directly rejected on 35 U.S.C 101 stands rejected due to its dependency.

To expedite a complete examination of the instant application, the claims rejected under 35 U.S.C 101(nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Response to Arguments

7. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-7, 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,757,882 to Chen et al. hereinafter "Chen".

Regarding claim 1, Chen discloses a method of matching selectable user module with a plurality of programmable resources associated with an integrated circuit (See the tool as shown in figure 4).

a. Displaying said selectable user module, wherein said user module is representation of a configuration of a programmable circuit (As illustrated, upon invocation, IP package processor 250 (more specifically, description reader 252) identifies and reads basic description 212, block 1302. Description reader 252

then stores the basic information read into corresponding data fields of database 260, block 1304 (Column 9, line 59- Column 10 line 3));

b. In response to a selection of said selectable user module, comparing a description of a hardware resource requirement of said selectable user module with a description of said plurality of programmable resources associated with said integrated circuit (Next, description reader 252 identifies and reads pins and bus related description 214, block 1308 Figure 13 (Column 10, lines 4-16)); and

c. identifying a first allowed programmable hardware resource on the integrated circuit satisfying the hardware resource requirement of said selectable user module (In response, bus compatibility analyzer 254 determines the bus architectures supported accordingly, including bus signals implemented, and disposition/handling of the unimplemented signals, block 1310 (Column 10, lines 4-16)).

Regarding claim 2 Chen discloses wherein the description of the hardware resource requirement of the user module is represented as XML (For the embodiment, description 210' is expressed using a XML-like Language having XML like language tags defined in accordance with a schema of a namespace associated with Tool Suite 204 (Column 8, lines 23-35)).

Regarding claim 3, Chen discloses wherein the description of the plurality of said selectable programmable resources are represented as XML data (For the embodiment,

description 210' is expressed using a XML-like Language having XML like language tags defined in accordance with a schema of a namespace associated with Tool Suite 204 (Column 8, lines 23-35)).

Regarding claim 4, Chen discloses the method according to Claim 1 further comprising highlighting the first allowed programmable hardware resource using a graphical user interface (Upon determining the information, in like manner, bus compatibility analyzer 254 stores the supported bus architecture information, including related synthesized information, into database 260, block 1312 along with figure 6).

Regarding claim 5, Chen discloses identifying a second allowed programmable hardware resource for use with the invention. Figure 7 shows a plurality of memory devices that satisfy the hardware resource of the core being used.

Claim 6 discloses a similar limitation to Claim 4 thus is rejected for the same reasons as claim 4.

Regarding claim 7, Chen discloses the method according to Claim 1 further comprising identifying a disallowed programmable resource on the integrated circuit wherein the disallowed resource represents an unavailable resource on the integrated circuit that otherwise satisfies the hardware resource requirement of the user module (In response, bus compatibility analyzer 254 determines the bus architectures supported

accordingly, including bus signals implemented, and disposition/handling of the unimplemented signals, block 1310 (Column 10, lines 4-16) when determining what is allowable the disallowed resources are identified.

Regarding claim 10, Chen discloses the method according to Claim 1 further comprising updating the description of the hardware resource requirement of said selectable user module

> (Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

Regarding claim 11, Chen discloses the method according to Claim 10 wherein said updating is performed in response to changes in a hardware resource requirement of said selectable user module.

> (Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

Regarding claim 12, Chen discloses the method according to Claim 1 further comprising adding an additional selectable user module to the description of the hardware resource requirement of said selectable user module.

(Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

Regarding claim 13, Chen discloses the method according to Claim 1 further comprising updating the description of the plurality of programmable resources associated with said integrated circuit

(Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

Regarding claim 14, Chen discloses the method according to Claim 13 further comprising adding an additional chip description to the description of the plurality of programmable resource associated with said integrated circuit

(Customizable attribute or parameter descriptions 1227 set forth between customizable attribute/parameter description tags 1230a and 1230b may include e.g. a number of IP component parameters to be resolved based directly or indirectly on user inputs 1227a-1227c and 1227d-1227f. Similarly to the customizable bus interface parameters, the descriptions may include identification of the IP component parameters, the manner of resolution, user prompts and so forth. Customization UI element descriptions 1231 set forth between customization UI element description tags 1226a and 1226b may include e.g. choices for a number of choice elements 1231a-1231c and 1231d-1231f. As described earlier, examples of choices may be "enabled" or "disabled" for an included timer. Fig. 18 Column 9, lines 18-31)

9. Claims 15, 18-24, 26-32 rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pre-Grant Publication No. 2002/0016706 to Cooke et al. hereafter, "Cooke."

Claim 15 recites the apparatus of method claim 18, thus is rejected for the same reasons as claim 18.

Regarding claim 18, Cooke discloses a computer implemented method of determining hardware resources for an electronic design

a) selecting an electronic design [block] represented as a user module [From the HDL or other high level description, the actual logic cell implementation is typically determined by logic synthesis, which converts the functional description of the block into a specific circuit implementation of the block. (Paragraph 36)];

b) accessing a data description of resources required for said user module [The computer 110 is preferably coupled to a mass storage device (e.g., magnetic disk or cartridge storage) providing a layout database 195 with which the foregoing system components interface (Paragraph 40)];

c) accessing data descriptions of a plurality of programmable resources of an electronic device [Floorplan footprints]; and

d) comparing said data description of said user rnodule with said data descriptions of said plurality of programmable resources to automatically determine potential placement options of said user module among said plurality of programmable resources [At each stage of the design process, as well as at the fabrication stage,

various tests may be run to ensure correct operability of the circuit design (Paragraph 36)].

Applicant Argues

The "blocks" of the reference are not equivalent to user modules. In particular "The selectable user module of the present invention is not such a chunk of circuitry because it contain information regarding the programming of a programmable circuit." And furthermore fails to show that they are displayed. Cooke et al. does not discuss matching programmable resources with the requirements of a selectable user module in any way.

Examiners Response

Examiner disagrees with Applicants assertion. Applicant is arguing from portions of Cooke ill suited to support Applicants assertion. Examiner agrees that Cooke describes systems and methods for designing as integrated circuit as does the claimed invention, in the background of Cooke's specification Paragraph 6 indeed specifies that there are pre-designed and pre-hardened circuit designs available. However, a closer inspection of Cooke's specification reveals that as Figures 2/3 show there is not simply a selection of blocks that become a fabricated circuit design and the blocks used are *modules that are a representation of a configuration of a programmable circuit.*

> Referring now to FIG. 2A, there is shown a block illustration of a simplified IC 200 before the design of the IC has been completed, wherein a foundation block 202 and a number of peripheral component blocks B1, . . . , B12 have been specified, but where the actual connections between blocks remain undetermined. In actual, more realistic integrated circuit designs, the integrated circuit 200 would be far more complicated. Paragraph 41

Rather the blocks as relied upon are portions of circuitry that may be dropped in to a circuit design much like Applicant's PSoC Designer show in Figure 5A. Finally, Examiner agrees with Applicant's assertion that when a circuit design is finished, it is ready for fabrication, however fails to see the relevance, the mere fact that the Cooke reference encompasses more subject material is not germane to the argument presented.

Lastly to Applicants allegation that Cooke does not match programmable resources with the requirements of the module in any way, further attention is drawn to paragraph 43

In this process 302, **component blocks are identified from a component library 306 to perform specific functions set out in the RTL file 301**. The component blocks are preferably predefined, and although one or more may be based on a customized design not stored or only recently stored within the library 306.(Cooke paragraph 43)

Regarding claim 19, Cooke discloses the method according to Claim 18 "further comprising:

displaying on a graphical user interface, a first potential placement of said potential placement options; and in response to a user selecting a next placement icon, displaying on said graphical user interface, a second potential placement of said potential placement options [The block placer 130 determines the placement of cells

within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Regarding claim 20, Cooke discloses the method according to Claim 19 "wherein potential placement options are displayed using visual attributes and wherein said electronic device is a programmable microcontroller device [Figure 2A Microcontroller item 200]" as claimed.

Regarding claim 21, Cooke discloses the method according to Claim 18 "wherein said user module requires one programmable resource to place [Figure 2A item B's]" as claimed.

Regarding claim 22, Cooke discloses the method according to Claim 18 "wherein said user module requires two programmable resources to place [Figure 2A item B's]" as claimed.

Regarding claim 23, Cooke discloses the method according to Claim 18 "wherein said plurality of programmable resources comprise a plurality of analog programmable resources and a plurality of digital programmable resources [The computer 110 may also comprise or be connected to mass storage containing one or more component libraries (not shown) specifying features of electrical components available for use in circuit designs (Paragraph 40)]" as claimed.

Regarding claim 24, Cooke discloses the method according to Claim 18 "wherein said comparing automatically prunes out programmable hardware resources that do not satisfy requirements of said user module

> [The block floorplanner 120 provides for the definition of block functions, block regions, and constraints on these for the purpose of interactive floorplanning operations by the circuit designer, and the control of placement operations of the block placer 130. The block placer 130 determines the placement of cells within blocks according to the constraints defined by the circuit designer. (Paragraph 38)]" as claimed.

Claims 26-32 recite the system of method claims 18-24, thus are rejected for the same reasons as claims 18-24

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of PSoC Designer: Integrated Development Environment User Guide Revision 1.09, hereinafter "Guide 1.09".

Regarding claim 8, Chen teaches the method according to Claim 7 further comprising distinguishing disallowed programmable resources. Chen does not

expressly teach highlighting the disallowed programmable resource using said graphical user interface.

Guide 1.09 teaches that if you attempt to select a User Module that requires more resources than are currently available, PSoC Designer will not allow the selection.

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to use the user feedback of disallowing the selection with the method of Chen.

The motivation for doing so would have been to give the user visual feedback for the operation being performed.

Regarding claim 9, the combination as applied to claim 9 does not expressly teach that the user feedback is highlighting in gray.

Examiner finds this limitation to be design choice, highlight in gray, or graying out is common and is the default for disallowed user feedback in Windows. Furthermore, the method could just have easily picked any other color for indication of such.

11. Claims 16, 17, 25, 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Cooke.

Claims 16, 17 recite the same limitations as claim 25. Thus claims 16 and 17 are rejected for the same reasons as claim 25.

Regarding claim 25 Cooke teaches the method according to Claim 18 wherein the descriptions are represented as data.

Cooke does not expressly teach that the data in the method takes the form of the XML data.

However, these differences from the prior art of record are only found in the nonfunctional descriptive material and do not make a meaningful contribution to the definition of the invention as recited. The limitation of XML does not alter how the method as described in the specification functions. Thus, the identified descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to use XML to store the data in Cooke.

The motivation for doing so would have been to allow the invention as disclosed to be used in various fields of endeavor as the data suggests (XML is a web based technology), thus such data does not alter how the invention functions and the subjective interpretation of the data does not patentably distinguish the claimed invention. For further evidence of this see Chen above.

Claim 33 recites similar limitations as claim 2, thus is rejected for the same reasons as claim 2.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form USPTO-892. In particular, examiner has become aware of Psoc Designer: Integrated Development Environment User Guide Revision 1.09 dated 5/30/2001. Since the features of this version look remarkably similar to those depicted in the figures of the instant application examiner suggests a review of the claimed subject matter vs. previous versions of this and related manuals up to applicants filing date.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LRO